Claims

[c1] A method of controlling cracks in an integrated circuit device comprising:
providing an integrated circuit having a crack stop along a perimeter of said integrated circuit;
forming at least one opening in a wiring level in said integrated circuit adjacent to said crack stop;
depositing a release material over said integrated circuit in an amount sufficient to at least fill said opening;
removing excess release material to form a vertical interface along said perimeter of said integrated circuit within said opening adjacent to said crack stop, thereby controlling cracks in said integrated circuit via said vertical interface and preventing said cracks from penetrating into said crack stop.

[c2] The method of claim 1 wherein said release material comprises a material having low adhesion strength to adjoining sidewalls to enable said vertical interface to control said cracks in said integrated circuit by deflecting said cracks away from said crack stop such that penetration of said crack into said crack stop is avoided.

[c3] The method of claim 2 wherein said material is selected

from the group consisting of a polymer, fluoropolymer, polyimide, a low-k material, SiLK®, methylsilsesquioxane, an organic without adhesion promoter, parylene, a field oxide, SiCOH, an organic without adhesion promoter, TEFLON®, and SiCN+SiCOH.

[c4] The method of claim 1 wherein said release material comprises a material having a sufficient toughness to enable said vertical interface to control said cracks in said integrated circuit by absorbing said cracks, thereby avoiding said cracks from penetrating said crack stop.

[c5] The method of claim 4 wherein said release material comprises a thermoplastic polymer.

[c6] The method of claim 1 wherein said vertical interface comprises a plurality of individual spacer structures throughout said integrated circuit.

[c7] The method of claim 6 wherein said integrated circuit further includes a non-ultra low-k dielectric such that said crack stop and a plurality interconnecting wirings reside within said non-ultra low-k dielectric, the method further comprising:
etching exposed portions of said non-ultra low-k dielectric of said integrated circuit to form a plurality of openings;

depositing said release material in an amount sufficient to fill said plurality of openings; and
etching said release material to form vertical interface comprising said plurality of individual spacer structures throughout said integrated circuit, whereby selected ones of said vertical interface are adjacent said crack stop for controlling cracks in said integrated circuit.

[c8] The method of claim 7 further comprising the steps of:
depositing a low-k material in an amount sufficient to fill any remaining gaps in said integrated circuit;
planarizing a surface of said integrated circuit to at least expose said vertical interface;
depositing a capping layer over a surface of said integrated circuit; and
repeating said steps until a final integrated circuit structure is achieved.

[c9] The method of claim 1 wherein said vertical interface comprises a release trench along said perimeter of said integrated circuit within said opening adjacent said crack stop.

[c10] The method of claim 9 wherein said integrated circuit further includes an ultra low-k dielectric such that said crack stop and a plurality interconnecting wirings reside within said ultra low-k dielectric, the method further

comprising:
depositing a resist material over a surface of said integrated circuit;
patterning said resist material to form a patterned resist having a channel opening adjacent to an outside perimeter of said crack stop;
depositing said release material in said amount sufficient to fill said channel opening; and
etching said release material to form said vertical interface comprising said release trench along said integrated circuit perimeter adjacent to said outside perimeter of said crack stop, said release trench for controlling cracks in said integrated circuit.

[c11] The method of claim 10 further comprising the steps of:
removing remaining patterned blockout resist;
depositing a low-k material in an amount sufficient to fill any remaining gaps in said integrated circuit;
planarizing a surface of said integrated circuit to at least expose said vertical interface;
depositing a capping layer over a surface of said integrated circuit; and
repeating said steps until a final integrated circuit structure is achieved.

[c12] The method of claim 9 wherein said release trench along said perimeter of said integrated circuit within said

opening adjacent said crack stop further includes a void in said release trench.

[c13] The method of claim 1 wherein said release layer is deposited to a thickness ranging from about 5nm to about 1000nm.

[c14] A method of controlling cracks in a integrated circuit device comprising:
providing an integrated circuit having an ultra low-k dielectric layer;
providing a crack stop within said ultra low-k dielectric layer along a perimeter of said integrated circuit;
locating said ultra low-k dielectric layer within a vertical channel adjacent said crack stop;
modifying said ultra low-k dielectric layer within said vertical channel adjacent said crack stop to form a self-aligned vertical interface; and
controlling cracks in said integrated circuit by said self-aligned vertical interface preventing said cracks from penetrating into said crack stop.

[c15] The method of claim 14 further including depositing a hard mask over said ultra low-k dielectric layer and patterning said hard mask to form an opening adjacent said adjacent said crack stop such that said ultra low-k dielectric layer within said opening is exposed for modify-

ing.

[c16] The method of claim 14 wherein said ultra low-k dielectric layer within said vertical channel adjacent said crack stop is modified by exposing said ultra low-k dielectric layer to radiation for locally alter physical properties of said ultra low-k dielectric layer.

[c17] The method of claim 16 wherein said physical properties of said ultra low-k dielectric layer are altered by collapsing said ultra low-k dielectric layer within said vertical channel to form a void in said vertical channel adjacent said perimeter of said crack stop to weaken adhesion of said ultra low-k dielectric layer to said crack stop to enable said self-aligned vertical interface to control said cracks in said integrated circuit by deflecting said cracks away from said crack stop such that penetration of said crack into said crack stop is avoided.

[c18] The method of claim 16 wherein said physical properties of said ultra low-k dielectric layer are altered by increasing toughness of said ultra low-k dielectric layer within said vertical channel to enable said self-aligned vertical interface to control said cracks in said integrated circuit by absorbing said cracks, thereby avoiding said cracks from penetrating said crack stop.

[c19] The method of claim 14 further including the step of repeating said steps until a final integrated circuit structure is achieved.

[c20] A crack stop structure located at a perimeter of an integrated circuit device, comprising:
an integrated circuit having a low-k dielectric layer;
a crack stop along a perimeter of said integrated circuit within said dielectric layer; and
a vertical interface along said perimeter of said integrated circuit adjacent said crack stop within said dielectric layer for controlling cracks in said integrated circuit by preventing said cracks from penetrating into said crack stop.